Fig.1

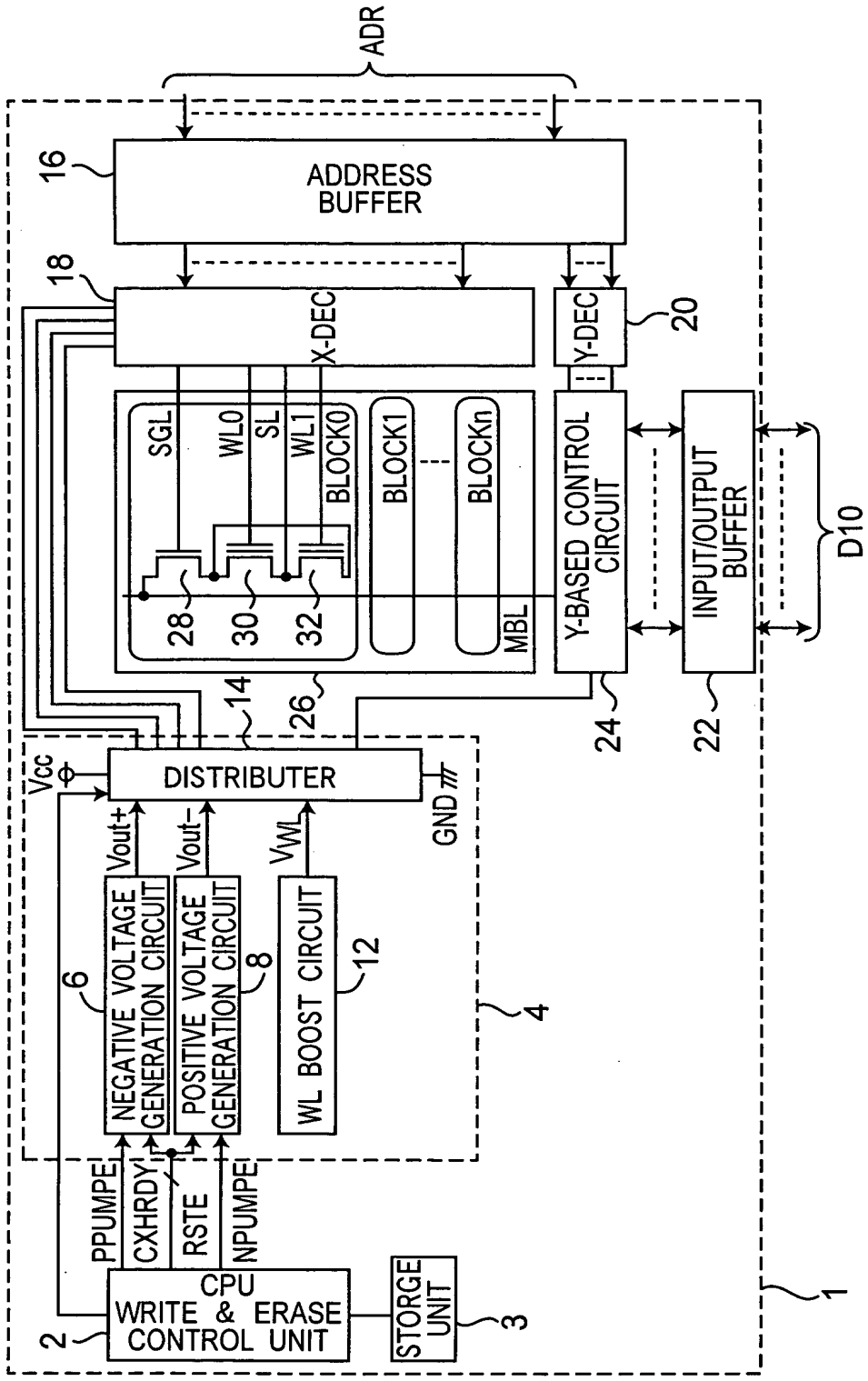

ADR
16
ADDRESS BUFFER
18
X-DEC
20
Y-DEC
SGL
WL0
SL
WL1
BLOCK0
BLOCK1
BLOCKn
MBL
28
30
32
Y-BASED CONTROL CIRCUIT
INPUT/OUTPUT BUFFER
D10
14
26
24
22
Vcc
DISTRIBUTER
GND
Vout+
Vout−
VWL
NEGATIVE VOLTAGE GENERATION CIRCUIT
POSITIVE VOLTAGE GENERATION CIRCUIT
WL BOOST CIRCUIT
6
8
12
4
PPUMPE
CXHRDY
RSTE
NPUMPE
CPU
WRITE & ERASE CONTROL UNIT
STORGE UNIT
2
3
1

Fig.2

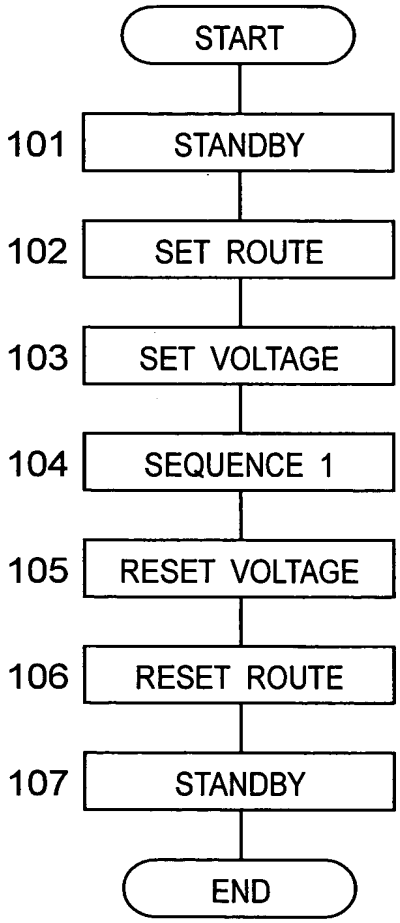

START
101
STANDBY
102
SET ROUTE
103
SET VOLTAGE
104
SEQUENCE 1
105
RESET VOLTAGE
106
RESET ROUTE
107
STANDBY
END

Fig.3

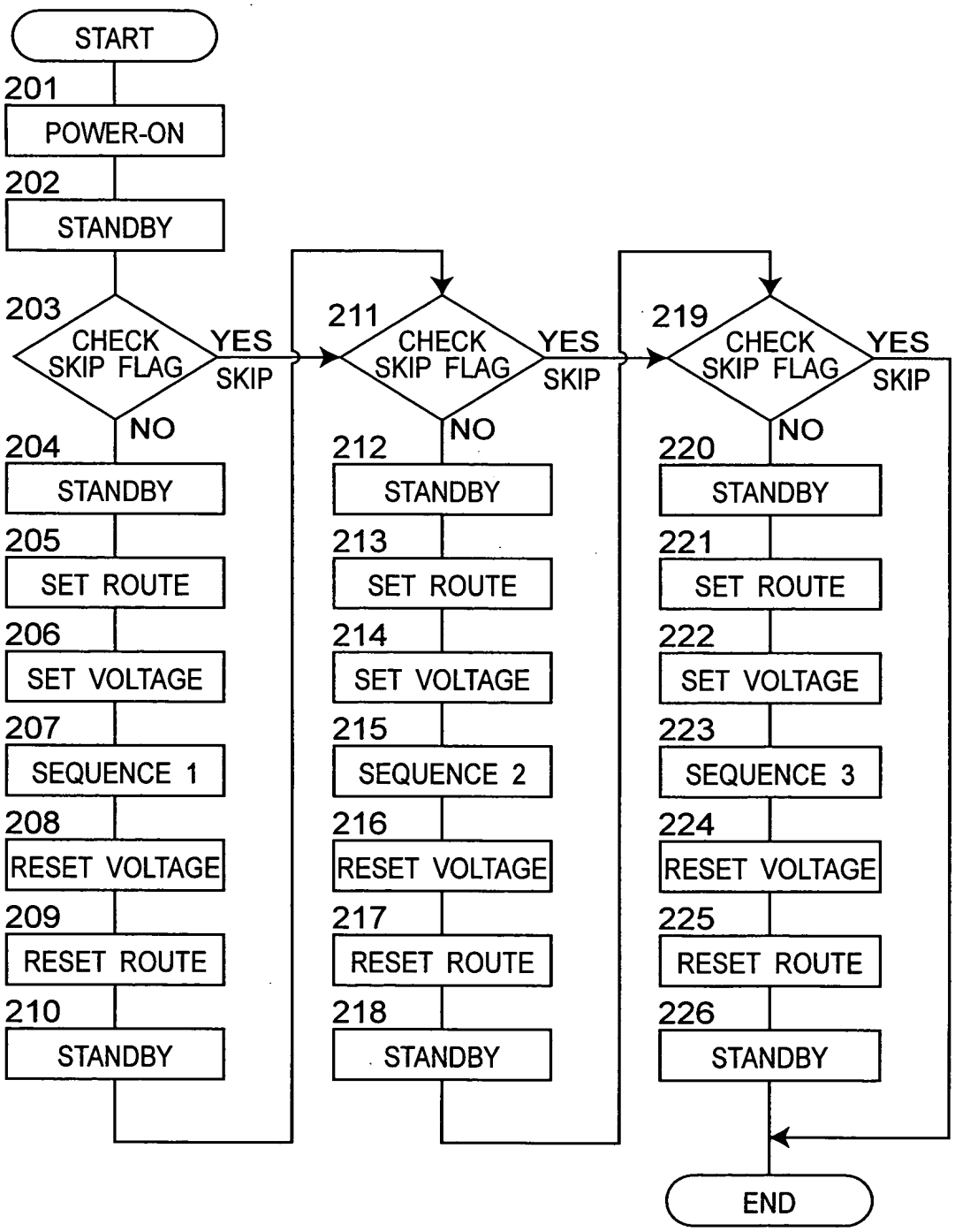

START
201
POWER-ON
202
STANDBY
203
CHECK SKIP FLAG
YES
SKIP
NO
204
STANDBY
205
SET ROUTE
206
SET VOLTAGE
207
SEQUENCE 1
208
RESET VOLTAGE
209
RESET ROUTE
210
STANDBY
211
CHECK SKIP FLAG
YES
SKIP
NO
212
STANDBY
213
SET ROUTE
214
SET VOLTAGE
215
SEQUENCE 2
216
RESET VOLTAGE
217
RESET ROUTE
218
STANDBY
219
CHECK SKIP FLAG
YES
SKIP
NO
220
STANDBY
221
SET ROUTE
222
SET VOLTAGE
223
SEQUENCE 3
224
RESET VOLTAGE
225
RESET ROUTE
226
STANDBY
END

Fig.4

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SKIP SEQUENCE 8	SKIP SEQUENCE 7	SKIP SEQUENCE 6	SKIP SEQUENCE 5	SKIP SEQUENCE 4	SKIP SEQUENCE 3	SKIP SEQUENCE 2	SKIP SEQUENCE 1

Fig.5

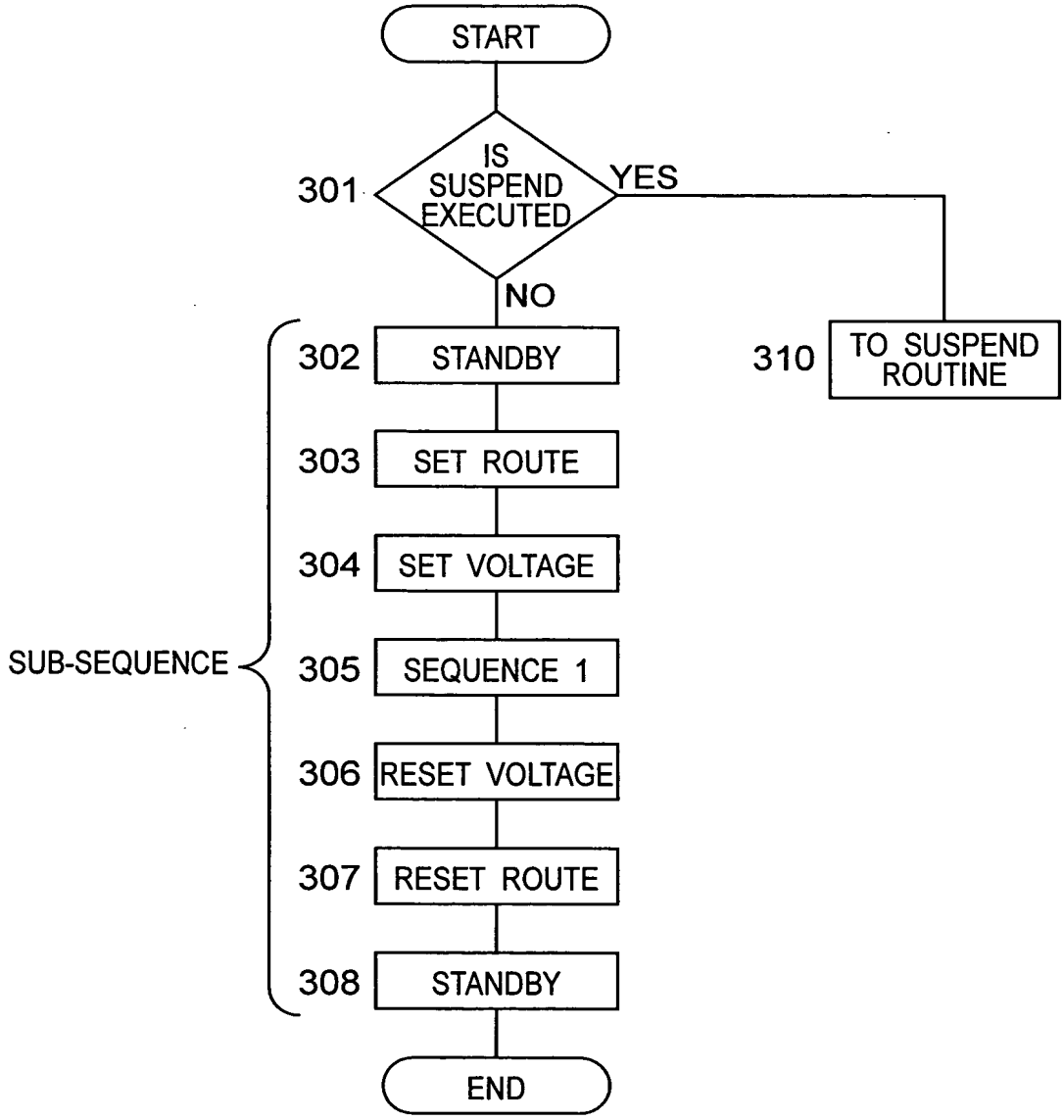
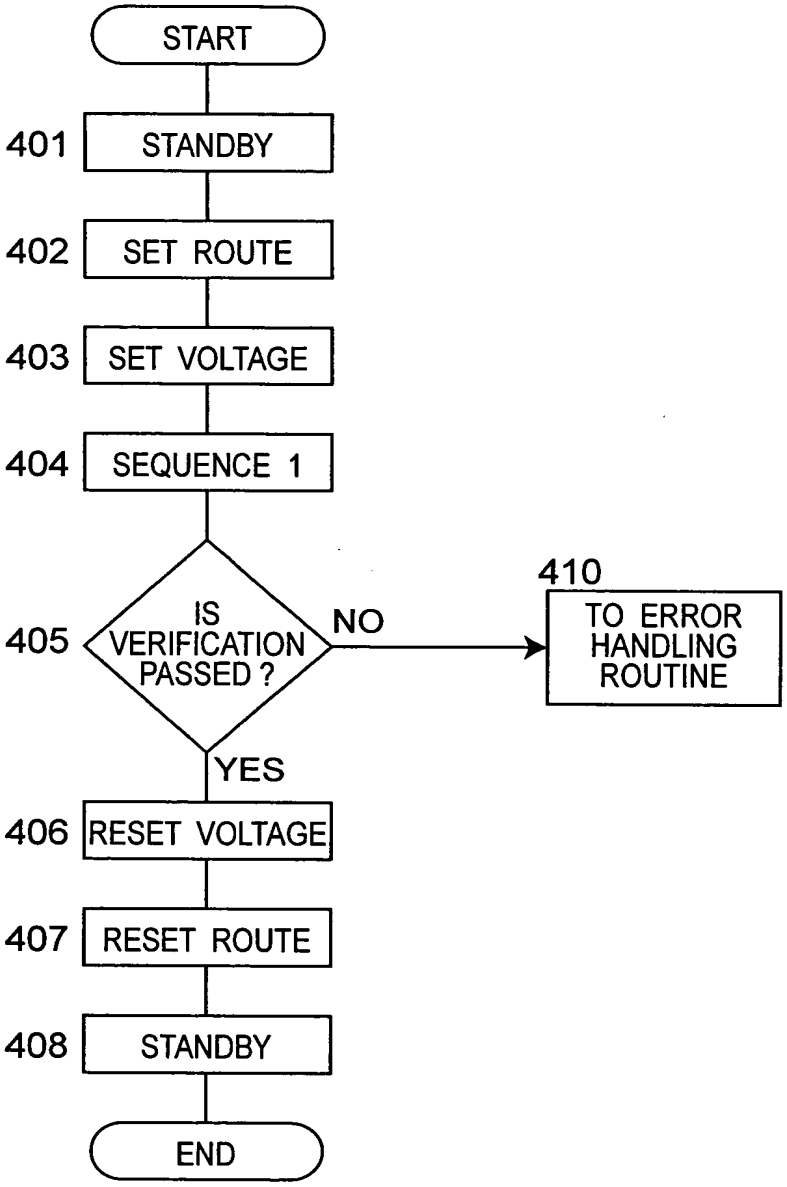

START
301
IS SUSPEND EXECUTED
YES
NO
310
TO SUSPEND ROUTINE
SUB-SEQUENCE
302
STANDBY
303
SET ROUTE
304
SET VOLTAGE
305
SEQUENCE 1
306
RESET VOLTAGE
307
RESET ROUTE
308
STANDBY
END

Fig.6


START
401
STANDBY
402
SET ROUTE
403
SET VOLTAGE
404
SEQUENCE 1
405
IS VERIFICATION PASSED ?
NO
410
TO ERROR HANDLING ROUTINE
YES
406
RESET VOLTAGE
407
RESET ROUTE
408
STANDBY
END